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Description

MULTIPLE DIELECTRIC FINFET STRUCTURE AND METHOD

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention generally relates to Fin-type field effect transistors (FinFET) and more particularly to an improved FinFET structure that includes multiple gate dielectric thicknesses.

[0003] Description of the Related Art

[0004] As the need to decrease the size of transistors continues, new and smaller types of transistors are created. One recent advance in transistor technology is the introduction of fin type field effect transistors that are known as FinFETs. U.S. patent 6,413,802 to Hu et al. (hereinafter "Hu patent"), which is incorporated herein by reference, discloses a FinFET structure that includes a center fin that has a channel along its center and source and drains at

the ends of the fin structure. A gate conductor covers the channel portion.

[0005] While FinFETs structures reduce the size of transistor-based devices, it is still important to continue to improve FinFETs. The invention described below provides a method and structure which improves the performance of FinFETs.

SUMMARY OF INVENTION

[0006] The invention provides a method of forming a fin-type field effect transistor (FinFET) structure that begins by patterning fins on a substrate and forming a first gate dielectric on the fins. Then, the invention protects first fins using a mask and removes the first gate dielectric from unprotected second fins. After removing the mask from the first fins, the invention forms an additional gate dielectric on the second fins and on the first gate dielectric that covers the first fins. This forms different thicknesses of gate dielectrics on the first fins when compared to the second fins. This process also forms multiple layers of dielectric over the first fins and forms the additional gate dielectric only over the second fins.

[0007] Processing steps used to complete the FinFET structure include doping ends of the fins to form source and drain regions separated by a central channel regions of the fins,

and forming a gate conductor over the channel regions. The gate dielectrics insulate the channel regions from the gate conductor.

[0008] The invention can utilize the fins in different types of transistors on the substrate. In this situation, one type of transistor would include gate dielectrics having a first thickness and a second type of transistor would include gate dielectrics having a second thickness different than the first thickness. Also, the invention can utilize the fins in multiple-fin transistors.

[0009] This process produces a fin-type field effect transistor (FinFET) structure that has different thickness gate dielectrics covering the fins extending from the substrate. These fins have a central channel region and source and drain regions on opposite sides of the channel region. Again, the thicker gate dielectrics can comprise multiple layers of dielectric and the thinner gate dielectrics comprise less layers of dielectric. A cap comprising a different material than the gate dielectrics can be positioned over the fins.

[0010] The use of different voltage ranges on separate regions of circuit areas (core, I/O, capacitors, etc.) requires different dielectric thickness to optimize device performance and

reliability. This invention proposes a multi-thickness dielectric FinFET structure and method to map this into future technologies. This invention uses multiple gate dielectrics on FinFET designs to optimize device performance/reliability and a method to fabricate them. By using a multiple dielectric design the invention avoids the density and performance penalties associated with complicated stacking schemes designed to keep device electric fields within the thinner dielectric imposed limits. This invention also extends the scaling capabilities of FINFETs.

[0011] These, and other, aspects and objects of the present invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the present invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

Brief Description of Drawings

[0012] The invention will be better understood from the following

detailed description with reference to the drawings, in which:

[0013] Figure 1 is a schematic diagram of a partially completed FinFET structure;

[0014] Figure 2 is a schematic diagram of a partially completed FinFET structure;

[0015] Figure 3 is a schematic diagram of a partially completed FinFET structure;

[0016] Figure 4 is a schematic diagram of a partially completed FinFET structure;

[0017] Figure 5 is a schematic diagram of a partially completed FinFET structure;

[0018] Figure 6 is a schematic diagram of a partially completed FinFET structure;

[0019] Figure 7 is a schematic diagram of a partially completed FinFET structure; and

[0020] Figure 8 is a flow diagram illustrating a preferred method of the invention.

DETAILED DESCRIPTION

[0021] The present invention and the various features and advantageous details thereof are explained more fully with reference to the non-limiting embodiments that are illustrated in the accompanying drawings and detailed in the

following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the present invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

[0022] As shown in Figure 5, one embodiment of the invention provides a fin-type field effect transistor (FinFET) structure that has different thickness gate dielectrics 502, 504 covering the fins 112-114 extending from the substrate 110. The thicker gate dielectrics 504 can comprise multiple layers of dielectric (200 and 500) and the thinner gate dielectrics 502 comprise less layers of dielectric (only 500). A cap 116 comprising a different material than the gate dielectrics can be positioned over the fins 112-114. As shown in Figure 6, the fins 66 have a central channel region covered by a gate conductor 64, and source 60 and drain 62 regions on opposite sides of the channel region.

[0023] Figures 1-5 illustrates one exemplary methodology uti-

lized to form the inventive structure. More specifically, Figure 1 illustrates fins 112-114 and caps 116 patterned on a substrate 110. Figure 2 illustrates a first gate dielectric 200 that is grown on the fins 112-114. Then, the invention protects first fins 114 using a mask 300, as shown in Figure 3. In Figure 4, the invention removes the first gate dielectric from unprotected second fins 112, 113. After removing the mask from the first fins (as shown and Figure 5), the invention forms an additional gate dielectric 500 on the second fins 112, 113 and on the first gate dielectric 200 that covers the first fins 114.

[0024] This forms different thicknesses of gate dielectrics 504 on the first fins 114 when compared to the thickness of the dielectrics 502 on the second fins 112, 113. This process also forms multiple layers of dielectric 200, 500 over the first fins 114 and forms only the additional gate dielectric 500 over the second fins.

[0025] As shown in Figure 6 and 7, additional processing steps, such as those described in the Hu patent are used to complete the FinFET structure. For example, the ends of the fins 66 are doped to form source 60 and drain 62 regions separated by a central channel region. Gate conductors 64 are formed over the channel regions of the fins

66. The gate dielectrics 200, 500 insulate the channel regions from the gate conductor 64.

[0026] While a limited number of types of FinFETs are shown in the drawings, one ordinarily skilled in the art would readily understand that the invention can utilize the fins in many different types of transistors on the substrate. For example, the invention can form complementary transistors on the same substrate, or can form transistors with different voltage requirements on different areas of the substrate. Therefore, in these situations, certain types of transistor would include gate dielectrics having a first thickness and other types of transistor could include gate dielectrics having a second thickness. Also, the invention can utilize the fins in multiple-fin transistors. Further, one ordinarily skilled in the art would clearly understand that the invention is not limited to only two different thicknesses of gate dielectrics. To the contrary, any number of gate dielectric thicknesses can be formed with the invention by simply repeating the masking and depositing processes shown in Figures 3-5.

[0027] Figure 8 illustrates the methodology of the invention in flowchart form. More specifically, in item 800, the invention patterns fins on a substrate and in item 802, the in-

vention forms a first gate dielectric on the fins. Then, the invention protects first fins using a mask (804) and removes the first gate dielectric from unprotected second fins 806. After removing the mask from the first fins, the invention forms an additional gate dielectric on the second fins and on the first gate dielectric that covers the first fins 808. This forms different thicknesses of gate dielectrics on the first fins when compared to the second fins. For example, one gate dielectric could be more than twice as thick as the other gate dielectric. This process also forms multiple layers of dielectric over the first fins and forms only the additional gate dielectric over the second fins. Forming n layers on one set of FINs, n-1 on another set, n-2 on a third set etc., so the process is repeatable and flexible. Processing steps used to complete the FinFET structure include doping ends of the fins to form source and drain regions 810 separated by a central channel regions of the fins, and forming a gate conductor over the channel regions 812.

[0028] In addition, while one methodology is discussed above, variations on this methodology are intended to be included within the invention. For example, while Figure 4 illustrates the removal of the first gate dielectric 200 from

selected fins, the inventive process can instead selectively retard oxide growth in one set of FINS (112 and 113) (for example by N2 implantation into the Fin sidewall) and then perform a single oxidation which would yield a first thickness on 112/113 and a second thickness (thicker film) on 114.Another aspect of the invention is that after growing layer 200 and protecting FINs 114 the invention etch off layer 200 on FINS 112-113. This has the effect of thinning the body of 112 and 113 as the grown oxide (200) consumes silicon during the growth phase. After layer 500 is grown the FIN bodies of 112 and 113 are thinner than 114 which is scaled in the correct direction, i.e. for higher voltages it is desirable to have a thicker oxide and thicker FIN body.

[0029] Additionally, any type of dielectric that functions properly as a gate dielectric can be used including oxides, nitrides, glasses, silicone, or any of the class of hi-K dielectrics etc. One ordinarily skilled in the art would understand that additional similar methodologies could be employed within the spirit and scope of the invention.

[0030] The use of different voltage ranges on separate regions of circuit areas (core, I/O, capacitors, etc.) requires different dielectric thickness to optimize device performance and

reliability. This invention discloses a multi-thickness dielectric FinFET structure and method to map this into future technologies. This invention uses multiple gate dielectrics on FinFET designs to optimize device performance/reliability and a method to fabricate them. By using a multiple dielectric design, the invention avoids the density and performance penalties associated with complicated stacking schemes designed to keep device electric fields within the thinner dielectric imposed limits. This invention also extends the scaling capabilities of FinFETs.

[0031] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.